

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**In re Application of:**

Kinsman et. al.

**Serial No.:** Not yet assigned

**Filed:** July 22, 2003

**For:** METHOD FOR FABRICATING A  
CHIP SCALE PACKAGE USING WAFER  
LEVEL PROCESSING AND DEVICES  
RESULTING THEREFROM

**Confirmation No.:** Not yet assigned

**Examiner:** Unknown

**Group Art Unit:** Unknown

**Attorney Docket No.:** 3572.2US  
(97-1243.02/US)

NOTICE OF EXPRESS MAILING

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Date of Deposit with USPS: July 22, 2003

Person making Deposit: Blake Johnson

**INFORMATION DISCLOSURE STATEMENT**

Mail Stop PATENT APPLICATION  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

The present application is a divisional of application Serial No. 09/917,127 filed July 27, 2001, pending, which is a divisional of application Serial No. 09/586,243, filed June 2, 2000, pending.

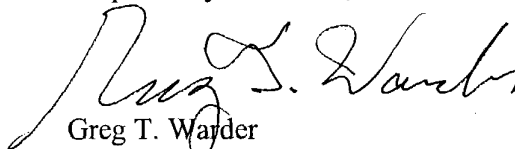
Pursuant to M.P.E.P. 2001.06(b), the Examiner is respectfully requested to consider the information of record in the prior applications, and to confirm in the first Office Action on the

**Attorney Docket No. 3572.2US (97-1243.02/US)**

merits that such art has in fact been reviewed. A PTO-1449 form listing all of the information of record in the prior applications is enclosed herewith.

This Information Disclosure Statement is filed within three (3) months of the filing date of the above-identified application, and no certification pursuant to 37 C.F.R. § 1.97(c) or a fee pursuant to 37 C.F.R. 1.17(p) is required.

Respectfully submitted,



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Date: July 22, 2003  
GTW/jml

Enclosure: Form PTO-1449

Document in ProLaw

Form PTO-1449  <b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b>  <i>(Use several sheets if necessary)</i>		Docket Number (Optional) <b>3572.2US (97-1243.02/US)</b>		Application Number <b>Not yet assigned</b>	
		Applicant <b>Kinsman t al.</b>			
		Filing Date <b>July 22, 2003</b>		Group Art Unit <b>Unknown</b>	

U.S. PATENT DOCUMENTS						
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	4,610,079	09/1986	Abe et al.			
	4,670,088	06/1987	Tsaur et al.			
	5,143,865	09/1992	Hideshima et al.			
	5,496,775	03/1996	Brooks			
	5,554,887	09/1996	Sawai et al.			
	5,703,406	12/1997	Kang			
	5,824,569	10/1998	Brooks et al.			
	5,834,843	11/1998	Mori et al.			
	5,844,779	12/1998	Choi			
	5,867,417	02/1999	Wallace et al.			
	5,908,317	06/1999	Heo			
	5,933,713	08/1999	Farnworth			
	5,969,426	10/1999	Baba et al.			

FOREIGN PATENT DOCUMENTS							
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO
	11-135663	05/1999	Japan			X	
	2000-133669 A	05/2000	Japan			X	

OTHER DOCUMENTS		(Including Author, Title, Date, Pertinent Pages, Etc.)
		Baliga, John, "Wafer-Level Packages to Include Solder Ball Support," Semiconductor International, November 2000, page 58.

EXAMINER	DATE CONSIDERED
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

Form PTO-1449  <b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b>  <i>(Use several sheets if necessary)</i>			Docket Number (Optional) <b>3572.2US (97-1243.02/US)</b>		Application Number <b>Not y t assigned</b>	
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U.S. PATENT DOCUMENTS						
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5,977,641	11/1999	Takahashi et al.			
	6,020,629	02/2000	Farnworth et al.			
	6,054,772	04/2000	Mostafazadeh et al.			
	6,077,380	06/2000	Hayes et al.			
	6,097,098	08/2000	Ball			
	6,107,164	08/2000	Ohuchi			
	6,137,164	10/2000	Yew et al.			
	6,150,717	11/2000	Wood et al.			
	6,153,448	11/2000	Takahashi et al.			
	6,181,569	01/2001	Chakravorty			
	6,208,018	03/2001	Ma et al.			
	6,297,553	10/2001	Horiuchi et al.			
	6,379,999	04/2002	Tanabe			

FOREIGN PATENT DOCUMENTS							
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO

OTHER DOCUMENTS			(Including Author, Title, Date, Pertinent Pages, Etc.)

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